A High Power On-Wafer Pulsed Active Load Pull System

by

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Abstract:

This paper describes a unique on-wafer load pull system that is capable of measuring load pull contours on true high power and large periphery devices. Measurements are made under low duty cycle pulsed DC and RF conditions to minimize the effects of heating due to power dissipation in the on-wafer environment. With the current implementation of the load pull system, any load impedance on the Smith chart can be presented to the output of four Watt devices. The system is fully error corrected for reflection coefficient, transmission coefficient, input power incident, input power delivered, and output power delivered. The system is capable of automatic control and measurement by means of a HP 9000 series workstation. Data taken on C band MMIC power amplifiers and 2mm GaAs FET's is presented.

Introduction:

Load pull systems are used to obtain design information on large signal, high power devices or to robustly verify the validity of nonlinear models for high power devices. The most desirable form of load pull information is data taken on devices that are still in wafer form using a microwave probe station. Unfortunately, previous approaches to load pull systems were ill suited for the on-wafer environment due to a variety of reasons. The passive load pull systems can not overcome the significant loss associated with microwave probe stations. This results in an inadequate range of load impedances that can be presented. The active load pull systems are not limited by the probe system loss. However, these systems are all based on cw measurements using a standard cw vector network analyzer. This cw operation is unacceptable for the on-wafer environment for devices that have gate widths more than 500 uM due to the high DC power dissipation and the poor heat sinking in wafer form. The load pull system presented here overcomes these limitations and uses a more complete error correction for impedance parameter, transmission parameter and power measurements. The main contributions demonstrated in this paper include:
1) An expandable active load pull approach that currently is capable of presenting any arbitrary load impedance at the device pads for devices that can deliver up to 4 Watts of power output in an on-wafer environment.
2) A pulsed DC and pulsed RF measurement environment that prevents the wafer form device from overheating due to power dissipation.
3) A programmable electronic approach to the adjustment of phase and amplitude for the "reflected" component of the effective load impedance.
4) A robust error correction scheme that utilizes vector error correction for input impedance, load impedance, insertion gain, power delivered to the input, power incident to the input and power delivered to the load.
This paper discusses the configuration of the on-wafer load pull system, the system considerations, the error correction approach, the presentation of data taken on the system and a discussion of future enhancements.

System Description:

The on-wafer pulsed active load pull is based on a variation of the Takayama active load pull system [2]. A simplified block diagram for the system is shown in figure 1. The load pull system uses separate 10 Watt TWTA 's for the input and the output of the system. This allows for adequate power to be made available for the output side of the system to obtain any effective load impedance on the Smith chart presented at the output side probe tip. The 10 Watt TWTA was experimentally verified to be sufficient to be able to provide arbitrary tuning to on-wafer devices that delivered up to 4 Watts of delivered power into their optimum impedance.
The second 10 Watt TWTA is used to provide the input drive for the system. This TWTA was experimentally verified to be sufficient to provide drive levels of up to +25dBm delivered to the input of the device in an untuned, 50 Ohm environment. It is critical to maintain a broadband, real impedance on the input side of the system to terminate any harmonics eminating from the input of the device in a "known" impedance. In this system, any harmonics from the input of the device will be terminated in approximately 50 Ohms by the isolator after the input TWTA. Any attempt at "helping out" the input TWTA by inserting an input tuner in the system results in nonrepeatable results under large signal conditions due to the highly reflective and arbitrary nature of the harmonic termination of the input tuner.
The heart of the measurement system is a HP 85108 pulsed vector network analyzer. This system includes a vector reciever with an IF bandwidth of 2.5 MHz to obtain maximum sensitivity under pulse

conditions and a high power mixer based test set that has expansion links that are used to install the additional hardware needed for the active load pull. In addition, the test set has been modified to incorporate a HP 71500 microwave transistion analyzer. The use of the transition analyzer is discussed in the discussion of future work. It was determined through experimental verification that a pulse width of 1 microsecond with a duty cycle of 10 % was appropriate to simulate a similar thermal environment on-wafer as would be obtained under cw conditions in a packaged environment with a proper heat sink. The standard HP 85108 pulse vector network analyzer is well suited to make accurate vector measurements under these pulse conditions. All the vector error correction for the ratio measurements is done utilizing the internal error correction capabilities of the HP8510C vector network analyzer.

In addition to the vector ratio measurements for the input impedance, load impedance and insertion gain, the HP8510C reciever is used to measure the absolute power at the input and output of the device under pulsed conditions. Each unratioed parameter, a1,a2,b1,b2, has been characterized for power linearity and correction factor to obtain the error corrected values that correspond to power incident on and reflected from the device under test and the power incident on and reflected from the load. When done in this fashion, the error coefficients for the power measurements are simple extensions of the normal 12 term error coefficients obtained for the ratio measurements.

Load pull contours can be generated for either conditions of constant incident input power or constant delivered input power. Delivered power is defined as the difference between the power incident and the power reflected in Watts. Incident power to the device under test has to be vector error corrected to account for the limited raw source match of the input side of the test system and the limited S12 of the device under test as a function of load impedance under large signal conditions. All the error correction for power is done remotely using computer control with an HP 9000 series workstation.

The pulse DC supplied for the device under test is provided by some custom hardware in the load pull system. The high current pulsed DC for the device drain is produced by means of a pulse modulator built by GE for a phase 3 MMIC project[7]. The pulsed DC is applied to the test system by means of a pair of modified bias tees. Both a "force" tee and a "sense" tee are used to account for Ohmic drops in the test system. The inductor feeds in the bias tees have been modified to decrease their inductance and increase their current handling capability. These special bias tees are available from Hewlett Packard as a special option on the standard bias tees. Pulsed currents of up to 10 Amps and voltages of up to 20 V can be supplied to the system.

In an active load pull system, the load impedance is synthesized by taking a portion of the input drive, amplitude and phase shifting the signal, amplifying it and sending it to the output of the device under test. This signal takes the place of the wave "reflected from the load" under passive conditions. The effective load impedance generated is measured in real time by the vector error corrected reflectometer on the output side of the load pull system. The phase and amplitude adjustment is traditionally done using electomechanical line stretchers and variable attenuators. These "tuning" elements are slow to automate and are subject to mechanical wear. The active load pull presented here utilizes a complete electronic approach to the tuning. It is believed that this is this first published use of this approach in an active load pull system. The phase and amplitude adjustment is performed by an I-Q vector modulator that is inserted at the input of the "load" TWTA. Since it is at the input of the TWTA, it does not have to withstand high power levels and any harmonics generated by the modulator are filtered by the low pass filter after the TWTA. Since the TWTA is operated in a more or less linear fashion, any amplitude or phase change at the input will be replicated on the output. Since the effective load impedance is measured in real time by the system, it is not necessary to "predict" the exact amplitude and phase change. A block diagram of the vector modulator is shown in figure 2. The phase and amplitude is changed in the modulator by means of DC levels applied to the I and Q inputs from two 10 bit bipolar DAC's. This type of modulator has greater than 20 dB of amplitude range and full 360 degree phase range.

Error Correction:

The systematic errors in the load pull system are all linear and time invariant. Upon inspection of the signal flow graphs for both a "standard S parameter" configuration and the active load pull configuration for the HP85108 pulse vector network analyzer, it is observed that the sources of the error coefficients are identical. The only differences occur when the calculations for "error corrected" data are performed. Therefore, the error coefficients for the system are extracted using the system in a "S parameter" configuration using a conventional on-wafer calibration (SOLT,TRL,LRM). Because of the nature of the modifications made to the system to use it as an active load pull, the network analyzer must be calibrated with the assistance of a computer. First, the raw data for each calibration standard measurement is performed and stored to disc. This step is necessary because the active load on the output of the system needs to be changed between the forward and reverse measurements. The "raw" standard data is then triggered into the HP 8510C using the SIMS command to perform a "simulated" calibration. The error coefficients are now available for the various error corrections.

Figure 3 shows some of the flow graphs that were used in the error correction. The input reflection coefficient is corrected in the traditional fashion. The load reflection coefficient error correction follows the same form as a traditional error correction except that the quantity that is corrected is (1/S22). The corrections for the power measurements are similar to those proposed by Tucker and Bradley [3] except that the error corrections for power incident to the device under test are also calculated. By proper input into the error correction matrix in the HP 8510B, all the ratioed measurements can be displayed fully error corrected. All the power measurements and corrections are done in the controlling computer.
All of the power measurements in the system are based on readings taken from the a1 "raw" data on the HP8510B combined with the error corrected S parameters of the device under test and the previously determined system vector error correction coefficients. The relationship between the absolute power incident on the system and the a1 "raw" readings (scaling factor) is derived from a 1 port coaxial vector error correction and a power meter measurement at a convenient coaxial measurement plane at the input of the system. Once this scaling factor is known, the power incident on the device under test is derived from the flow graph analysis shown in figure 3 , the two port on wafer vector error correction coefficients and the error corrected value for S11 of the device under test. The power incident on the load will simply be this power incident on the device under test multiplied by the square of the error corrected value of S21 for the device under test. The power delivered to the load is determined from the power incident on the load combined with the measured corrected reflection coefficient of the load. The flow graph for the error correction of the load reflection coefficient is also shown in figure 3. In this way, all the pertinent power levels and the input reflection coefficient, the load reflection coefficient and the forward transmission coefficient are determined from "forward" measurements and one "raw" parameter measurement.

Measured Results :

Several devices were chosen to check out the load pull system. The first verification measurement was a very short thru connection (1 pS). The input reflection coefficient reference plane was extended to be the same as the output "load reflection coefficient" reference plane. It was then verified that both reflection coefficient measurements were identical at all settings of the active load. At the time the data was taken, the contour plotting routines were still in development so the contours were drawn by hand from the recorded data points. After operation of the system was verified, a 2mm wide GaAs FET was selected to be measured on the load pull system. Figure 4 shows the results taken on one of the 2mm FET's. The input frequency was chosen to be 5.5 GHz with a delivered input power level of +20 dBm. The drain voltage was set to 12 V and the gate was adjusted for 75% of IDSS. The pulse width was 1uS with a 10% duty cycle. The device delivered +29.96 dBm into the optimum impedance.
Another device that was measured on the on-wafer system was a C band high power amplifier MMIC. This part was designed to be terminated in a 25 Ohm load impedance. The results of the measurement are shown in figure 5. The input frequency was chosen to be 5.25 GHz with a power incident on the input of +20 dBm. Vds was set at 8V and the bias was pulsed with a 1uS pulse width and a 10% duty cycle. The maximum power delivered for this part was +36.74 dBm into an impedance very close to 25 Ohms.

Future Work:

The future work on the on-wafer pulsed active load pull includes completing the contour generation routines and extending the system to do on-wafer pulsed active harmonic load pull measurements. The heart of the harmonic load pull effort is the HP 71500 microwave transition analyzer. This instrument can make vector measurements of a pulsed signal at the carrier fundamental frequency as well as the first several harmonics up to 40 GHz. The active harmonic load will be configured in a fashion similar to that presented by Larose et.al. [4].

References:

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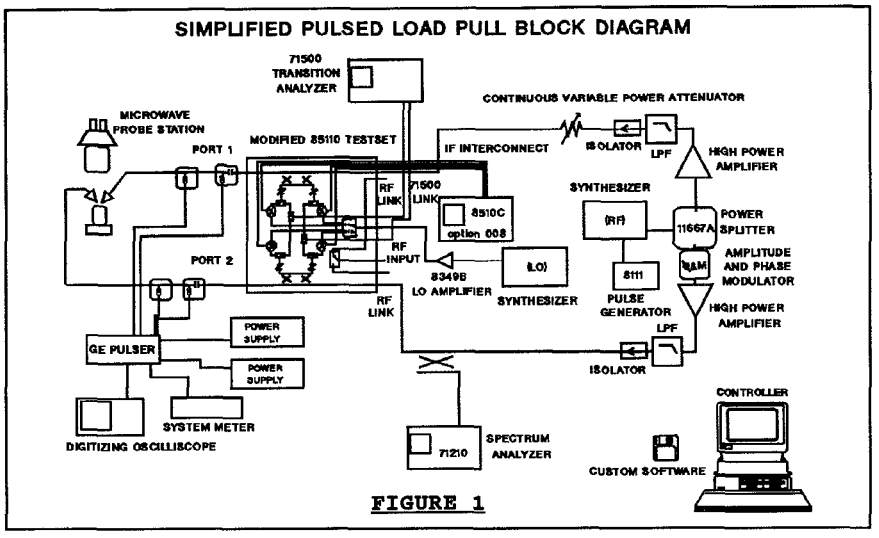

FIGURE 1

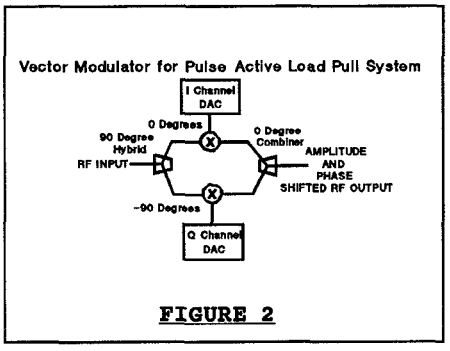

FIGURE 2

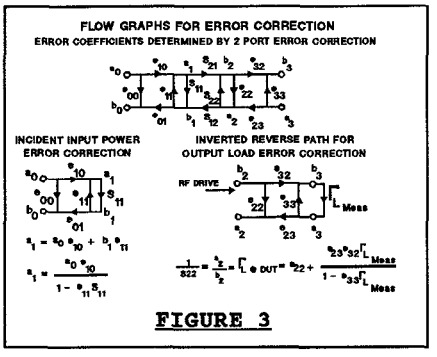

FIGURE 3

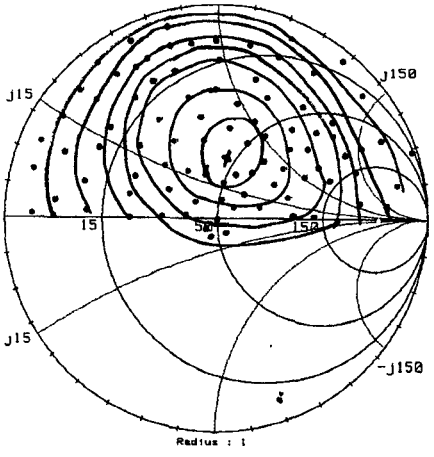

FIGURE 4

2mm GaAs FET:Pin=+20dBm Pout max=+29.96dBm
Freq.= 5.5 GHz Vds=12V Ids= 75% Idss
Pulse Width= 1uS Duty Cycle=10%
1dB Contours

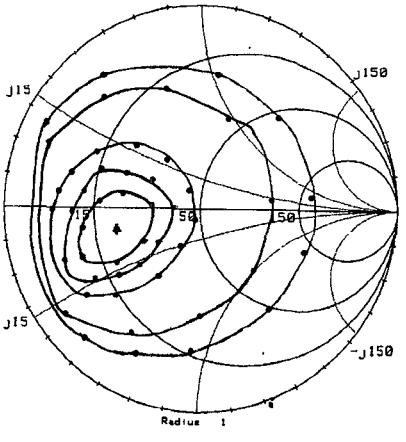

FIGURE 5

C Band HPA: Pin=+20dBm Pout max=+36.74dBm
Freq.= 5.25 GHz Vds=8V
Pulse Width=1uS Duty Cycle=10%
1dB Contours